Bit Constraint Parameter Decision Method for CDMA Digital Demodulator

Kyungtae Han, Iksu Eo, Kyungsu Kim and Hanjin Cho

Communication Digital IC Team, Micro-Electronics Technology Laboratory
Electronics and Telecommunications Research Institute.
161 Kajong-dong, Yusong-Gu, Taejeon, Korea, 305-350
E-mail: {han, iseo, kimks, hjcho}@etri.re.kr

Abstract-Bit constraint parameters of the digital demodulator for the code division multiple access (CDMA) system are modeled. We examined the bit constraint effect by measuring output signal-to-noise ratio (SNR). A performance-oriented method for optimizing the number of bits is proposed. We evaluated the bit constraint system by alternatively measuring output SNR and frame error rate (FER). Results demonstrate that this system with the optimal bit sets achieves FER performance within 3% in an additive white Gaussian noise channel at 3.8dB Eb/Nt. We found that the output SNR of 0.805 satisfy this CDMA requirement.

I. INTRODUCTION

Typical demodulators are implemented with analog block in front of the Analog Digital Converter (ADC) block as shown Fig. 1- (a). As the speed of the ADC is increasing, analog parts have been replaced with digital parts in communication systems [1]. In digital implementation, the reduction of the number of bits can save the total area that is related to the cost. However, if the number of bits is too small, the performance would be degraded.

Much research has been conducted for optimizing the signal wordlength of time-invariant digital filters using analytical time-domain, or frequency-domain analysis [2][3]. The simulation-based optimization method has also been studied for digital signal processing system using the cost-oriented optimization [4]. The method showed us the bit set of the lowest cost in the system, but a lot of simulation was required if the difference of the cost at each block would be large.

The bit constraint parameter needs to be designed to satisfy the minimum requirement of FER in the CDMA system [5]. But, it is very difficult to measure FER directly because at least 10^5 data bit simulations are required. Many researches have measured the output SNR to see the performance tendency.

In this paper, we replaced the analog demodulator with the digital demodulator as shown in Fig. 1. We proposed a performance-oriented optimization that reduced the number of simulations during the optimization. We also measured the output SNR to search the optimum number of bits, and then verified them with measuring the FER in order to save the total time of simulation. Finally, we induced the relation between the output SNR and the FER. It can evaluate the system performance of CDMA systems only with the measurement of the output SNR.

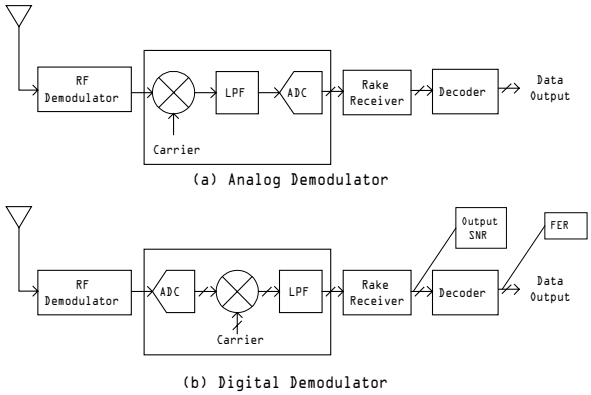


Fig. 1. Analog and digital IS-95A receiver.

II. DIGITAL DEMODULATOR

The demodulator converts a modulated signal into baseband signal. Digital demodulator reduces the system complexity as compared with an analog demodulator. In the digital demodulator block of Fig. 2, the sampled data at the ADC, are multiplied by a carrier signal down to the baseband signal and removed the outband signal by the low pass filter (LPF). The bit constraint parameters in the digital demodulator are as below:

- Bi: the number of input data bits

- Bc: the number of carrier data bits
- Bm: the number of multiplier output bits
- Bf: the number of filter output bits
- Bfc: the number of filter coefficient bits

The proper number of bits in each block has to be selected to satisfy the system requirements.

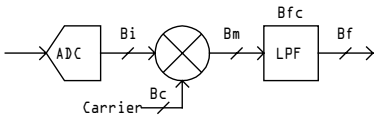


Fig. 2. Digital demodulator block.

III. BIT CONSTRAINT EFFECT

A. Performance Measurement

In the CDMA system, the performance of the demodulation of forward traffic channel in an AWGN environment is determined by the FER. It is difficult to measure the FER directly because at least 10^5 data bit simulations are required. On the other hand, the FER can be evaluated if the output SNR is known. The SNR estimation method used in our simulations is given by [6][7]

$$SNR = 10\log_{10}\frac{\hat{\mu}^2}{(2\hat{\sigma}^2)} \qquad (1)$$

where

$$\hat{\mu} = \frac{1}{n}\sum_{i=1}^{n}|x_i| \qquad (2)$$

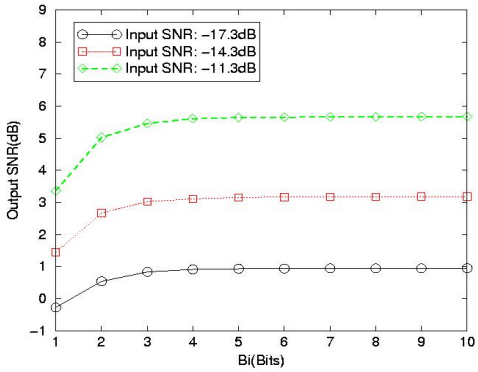
$$\hat{\sigma}^2 = \frac{1}{n-1}\sum(|x_i| - \hat{\mu})^2 \qquad (3)$$

and x_i is the I-channel output samples of the rake receiver in Fig. 1.

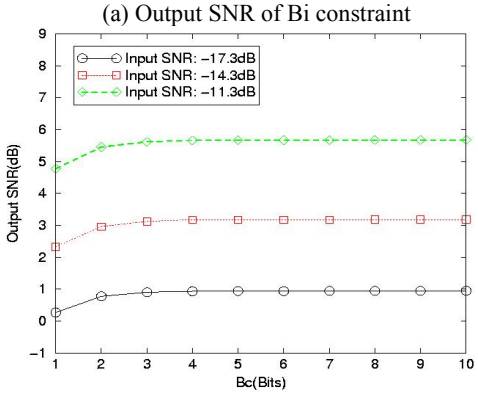
B. Bit Constraint

We varied the number of bits of one block leaving the other blocks unchanged and measure the output SNR. The results are shown in Fig. 3. Only the block was increased from one bit to ten bits while other blocks remained 32 bits. As the number of bit was increased, the output SNR was saturated to the certain value that would be the same as without any bit constraint. That meant it was needless to increase the number of bits over a certain point, called a critical point. The critical point of the Bi was about four bits and that of Bc, Bm, Bf and Bfc was about two, five, six, and six respectively.

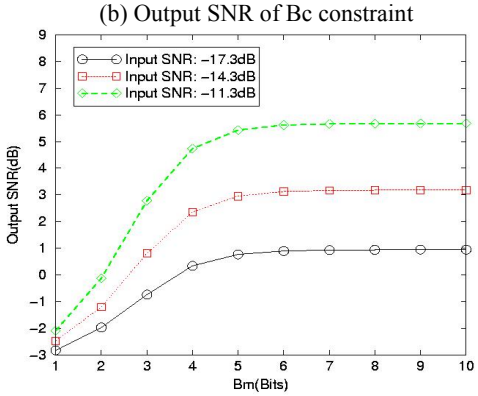
Result of the one-block constraint showed the tendency of the each constraint according to its bit. We can decide the critical bit that is the minimum bit to satisfy requirements. However, those set may not be the optimum bit set because those bits are the result without considering the other block's bit constraint. Therefore an all-block constraint simulation, which simultaneously constrained all block, needed to find out the optimum bit set.



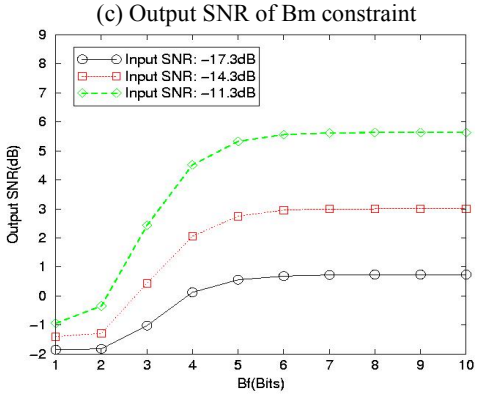
(a) Output SNR of Bi constraint



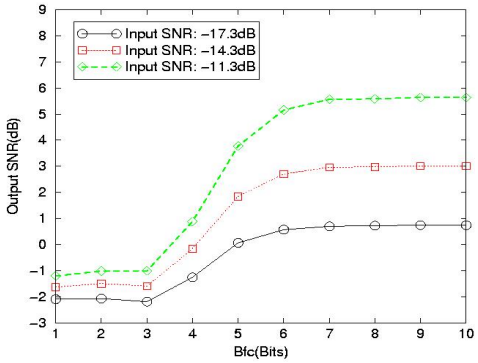
(b) Output SNR of Bc constraint



(c) Output SNR of Bm constraint



(d) Ouput SNR of Bf costraint



(e) Output SNR of Bfc constraint

Fig. 3(a)-(e). Output SNR results of one-block constraint

IV. OPTIMIZATION

A. Optimization Algorithm

In optimization algorithm, first we found out the critical bit set using one block constraint. Second, we increase the number of bits starting from the critical bit set until the system satisfied the requirements. The paper [4] optimized digital systems using a cost-oriented simulation, that increased number of bit for the lowest chip area. In that method, it would find the lowest cost bit set. But, if the difference of the cost at each block is large, the number of bits of only a low cost block may be increased.

In this paper, we proposed a performance-oriented simulation, which equally increased number of bit for the best performance rather than the low cost. It meant measuring the performance gradient during the bit constraint simulation and tracking the bit sets toward the best performance among the simulation results. Results may not be the lowest cost bit sets, but can be the lowest number of simulation and save the number of simulation.

The number of bit are optimized with measuring the output SNR and are evaluated the requirement of the CDMA system by measuring FER in order to save the simulation time. There are three stages in this simulation method as shown in Fig. 4. The first stage finds the critical bits from the one-block constraint simulation measuring the output SNR. In the second stage, increasing the number of bit at each block simulates the all-block constraint. And, the bit set from the result of maximum performance is updated to a new critical bit set. In the third stage, if the bit set is not satisfying with the minimum requirement of the FER, the stage II would be repeated. The final bit set could be the optimum bit set.

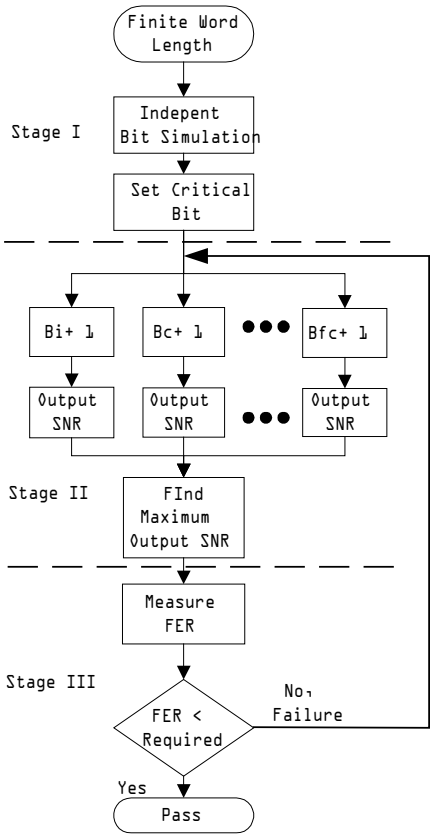


Fig. 4. Flow chart of the search for optimum bits

For example, the result is shown in table 1. The test parameters are set as:[5]

- Traffic Channel Rate Set 1 in AWGN
- Input SNR = -17.3 dB
- Eb/Nt = 3.8
- Rate= 9600 bps
- Required Performance: FER < 0.03

First, we took the critical bits 4,2,5,6,6 from the one-block constraint simulation. We increased one bits from each block, measured the output SNR and searched the bit set of the maximum performance. In this simulation, we found out that the multiplier output block (Bm) had the maximum output SNR of 0.449. So, we selected the bit set of 4,2,6,6,6 and measured the FER. Because the test result was not satisfied with the desired performance of 0.03, we repeated the stage II until the FER was under 0.03. Finally, we found 4,3,7,7,7 was optimum bit set.

B. Minimum Output SNR

The FER is usually used to measure the system performance, but it takes relatively long time to simulation. However, the output SNR spends less time than FER. The relation between the measured output SNR and the FER are plotted in Fig. 5. From the result, the output SNR of 0.805 is

the minimum output SNR to satisfy this CDMA requirement. Therefore, this output SNR could simply evaluate the CDMA demodulator system without measuring the FER.

C. Additional Optimization

There are two additional optimization algorithms in this method to save the simulation time and cost. First, if the step size is adaptively changed, it would reduce the number of the simulation. Second, if not only the performance-oriented optimization but also the cost-oriented optimization were simultaneously achieved, it would bring the low cost and fast optimization.

Table 1. Search sequence for the optimum word length.

Stage	Bi	Bc	Bm	Bf	Bfc	Output SNR	FER	Result
I	4	2	5	6	6	-	-	-
II	5+	2	5	6	6	0.283	-	-
II	4	3+	5	6	6	0.388	-	-
II	4	2	6+	6	6	0.449	-	Max
II	4	2	5	7+	6	0.376	-	-
II	4	2	5	6	7+	0.358	-	-
III	4	2	6+	6	6	0.449	0.150	Fail
II	5+	2	6	6	6	0.461	-	-
II	4	3+	6	6	6	0.544	-	Max
II	4	2	7+	6	6	0.515	-	-
II	4	2	6	7+	6	0.502	-	-
II	4	2	6	6	7+	0.521	-	-
III	4	3+	6	6	6	0.544	0.096	Fail
.....								
II	5+	2	6	7	7	0.780	-	-
II	4	3+	6	7	7	0.780	-	-
II	4	2	7+	7	7	0.805	-	Max
II	4	2	6	8	7	0.778	-	-
II	4	2	6	7	8+	0.749	-	-
III	4	3	7+	7	7	0.805	0.029	Pass

+: increasing bit

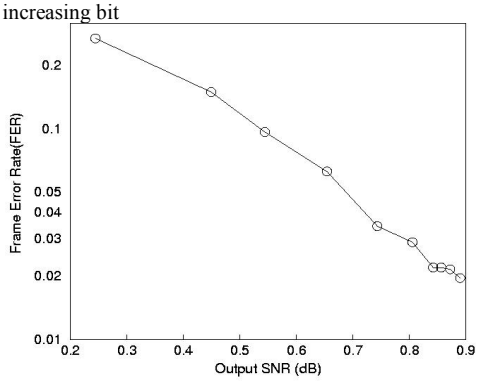


Fig. 5. Simulation results between the output SNR and the FER

V. CONCLUSION

Bit constraint parameters of the digital demodulator for the CDMA system are modeled. We evaluated the bit-constrained system by alternatively measuring output SNR and FER. It reduces simulation time comparing with measuring only FER. The proposed performance-oriented method is more effective than a cost-oriented method in searching for the optimal number of bits. Results demonstrate that this system with the optimal bit sets achieves FER performance within 3% in an additive white Gaussian noise channel at 3.8dB Eb/Nt. And we found that the output SNR of 0.805 satisfy this CDMA requirement. An adaptive bit step size and cost-performance oriented method would also reduce the simulation time and save the cost.

REFERENCES

[1] J. A. Wepman, "Analog-to-digital converters and their applications in radio receivers," *IEEE Comm. Magazine ,* Vol. 33, pp. 39-45, May 1995.

[2] L. B. Jackson, "On the interaction of roundoff noise and dynamic range in digital filters," *Bell Syst. Tech. J.,* pp. 159-183, Feb. 1970.

[3] F. Catthoor, J. Vandewalle, and H. He Man, "Simulated anneling based optimization of coeffieient and data word-lengths in digital filters," *Int. J. Circuit Theory Applications*, vol. 16, pp. 371-390, Sept. 1988.

[4] W. Sung and K. Kum, "Simulation-based word-length optimization method for fixed-point digital signal processing systems," *IEEE Transactions on Signal Processing*, Vol. 43, pp. 3087–3090, Dec. 1995.

[5] PN-3385, Page-Recommended Minimum Performance Requirements for 1.8 to 2.0 GHz Code Division Multiple Access (CDMA) Personal Stations.

[6] B. Y. Chung, C. Chien, H. Samueli and R. Jain, "Performance analysis of an all-digital BPSK direct-sequence spread-spectrum IF receiver architecture," *IEEE Journal on Selected Areas in Communications*, Vol. 11, pp. 1096-1107, Sept. 1993.

[7] J. K. Holmes, *Coherent Spread Spectrum System.* New York: Wiley, 1982.